Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims.

Listing of Claims

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1. (Currently Amended) A method of fabricating a semiconductor integrated circuit, comprising:

providing a dielectric portion;

reactive ion etching the dielectric portion, within a dielectric etch chamber to produce a feature having sidewalls and a bottom;

during said etching step, providing on the feature a metallic liner material to produce a metal-lined feature, the metallic liner being produced on the sidewalls and the bottom of the feature; and

depositing a conductive material on the lined feature.

2. (Cancelled)

3. (Currently Amended) The method of Claim 1, ~~wherein said etching step includes reactive ion etching, wherein said liner is a metallic liner, and~~ wherein said liner providing step includes redepositing sputter products from a metal hardmask during said reactive ion etching step.

4. (Original) The method of Claim 3, wherein said reactive ion etching step includes using a fluorocarbon gas.

5. (Original) The method of Claim 4, wherein the fluorocarbon gas is CF_4.

6. (Original) The method of Claim 3, wherein the metal hardmask is TaN.

7. (Original) The method of Claim 6, wherein said reactive ion etching step includes using a fluorocarbon gas.

8. (Original) The method of Claim 1, wherein the dielectric portion includes a low-k dielectric.

9. (Original) The method of Claim 1, wherein the dielectric portion includes an organic dielectric.

10. (Original) The method of Claim 1, including providing a seed layer on the liner material before said depositing step.

11. (Original) The method of Claim 1, wherein said conductive material is copper.

12. (Original) The method of Claim 1, wherein the feature is one of a trench and a via hole.

13. (Original) The method of Claim 1, wherein said etching step includes reactive ion etching, said reactive ion etching step including using a TEL SCCM etch tool.

14. (Currently Amended) The method of Claim 1, wherein said etching step includes transferring a pattern of a metal hardmask to ~~etching through~~ a dielectric hardmask of the dielectric portion and etching the pattern into the dielectric portion, said step of transferring the pattern to ~~etching through~~ the dielectric hardmask including using pressure in a range of 30 mT-100mT, using total RF power above approximately 800 watts, using an Ar flow rate in a range of 350-700 sccm, using an O_2 flow rate in a range of 10-30 sccm, and using one of a CF_4 flow rate in a range of 10-45 sccm and a CHF_3 flow rate in a range of 10-45 sccm.

15. (Currently Amended) The method of Claim 14, wherein said etching the pattern into the dielectric step includes etching an organic dielectric of the dielectric portion, said step of etching the organic dielectric including using an etch gas that is a mixture of N_2 at a flow rate of approximately 300 sccm and H_2 at a flow rate of approximately 300 sccm, and using a total RF power of approximately 3000 watts.

16. (Currently Amended) A semiconductor integrated circuit ~~fabricated according to the method of Claim 1~~, comprising:

a dielectric portion having a feature etched thereon using reactive ion etching in a dielectric etch chamber;

etching the dielectric portion, with a reactive ion etching within a dielectric etch chamber to produce a feature having sidewalls and a bottom;

a metallic liner lining at least two sidewalls and a bottom of the feature, the metallic liner being produced on the feature in the dielectric etch chamber during the reactive ion etching; and

a conductive material deposited on the lined feature.

17. (Currently Amended) A method of fabricating a semiconductor integrated circuit, comprising:

providing a dielectric portion;

in an etch chamber, reactive ion etching the dielectric portion to produce a feature having sidewalls and a bottom;

in said etch chamber, providing on the feature a metallic liner material to produce a metal-lined, the metallic liner being produced on the sidewalls and the bottom of the feature; and

depositing a conductive material on the lined feature.

18. (Currently Amended) The method of Claim 17, ~~wherein said etching step includes reactive ion etching, wherein said liner is a metallic liner, and~~ wherein said liner providing step includes redepositing sputter products from a metal hardmask during said reactive ion etching step.

19. (Currently Amended) The method of Claim 17, wherein said etching step includes transferring a pattern of a metal hardmask to ~~etching through~~ a dielectric hardmask of the dielectric portion and etching the pattern into the dielectric portion, said step of transferring the pattern to ~~etching through~~ the dielectric hardmask including using pressure in a range of 30 mT-100mT, using total RF power above approximately 800 watts, using an Ar flow rate in a range of 350-700 scan, using an 0_2 flow rate in a range of 10-30 sccm, and using one of a CF_4 flow rate in a range of 10-45 sccm and a CHF_3 flow rate in a range of 10-45 sccm.

20. (Currently Amended) The method of Claim 19, wherein said etching the pattern into the dielectric step includes etching an organic dielectric of the dielectric portion, said step of etching the organic dielectric including using an etch gas that is a mixture of N_2 at a flow rate of approximately 300 scan and H_2 at a flow rate of approximately 300 sccm, and using a total RF power of approximately 3000 watts.

21. (Currently Amended) A semiconductor integrated circuit ~~fabricated according to the method of Claim 17~~, comprising:

a dielectric portion having a feature with at least two sidewalls and a bottom, the feature being produced in the dielectric in an etch chamber according to a reactive ion etching;

a metallic liner on the sidewalls and the bottom of the feature, the metallic liner being produced in said etch chamber during the reactive ion etching; and

a conductive material deposited on the feature.

22. (Currently Amended) A method of fabricating a semiconductor integrated circuit, comprising:

providing a low-k dielectric portion;

reactive ion etching the low k dielectric portion, within a dielectric etch chamber to produce a feature having sidewalls and a bottom;

during said reactive ion etching step, providing on the feature a metallic liner material to produce a metal-lined feature, the metallic liner being produced on the sidewalls and the bottom of the feature; and

depositing copper on the lined feature.

23. (Currently Amended) A semiconductor integrated circuit ~~fabricated according to the method of Claim 22~~, comprising:

a low-k dielectric portion having a feature defining sidewalls and a bottom, the feature being produced in the low-k dielectric portion within a dielectric etch chamber according to reactive ion etching;

a metallic liner being produced on the sidewalls and the bottom of the feature to during said reactive ion etching; and

copper deposited on the lined feature.

24. (Currently Amended) A method of fabricating a semiconductor integrated circuit, comprising:

providing a low k, dielectric portion;

in an etch chamber, reactive ion etching the low k dielectric portion to produce a feature having sidewalls and a bottom;

in said etch chamber, providing on the feature a metallic liner material to produce a metal-lined feature, the metallic liner being produced on the sidewalls and the bottom of the feature; and

depositing copper on the lined feature.

25. (Currently Amended) A semiconductor integrated circuit ~~fabricating according to the method of Claim 24~~, comprising:

a low k, dielectric portion having feature with sidewalls and a bottom, the feature being produced in an etch chamber during a reactive ion etching of the low k dielectric portion;

the metallic liner on the sidewalls and the bottom of the feature, the metallic liner being produced in said etch chamber; and

copper deposited on the lined feature.